



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Rene Vangemert
Frank Worrell
Gagan V Gupta

Serial No. : 09/729,508
Filed : December 04, 2000
For : CPU Load-Miss Recovery
Mechanism

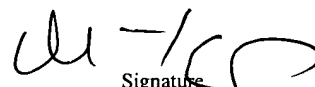
Group Art Unit : 2183
Examiner : Gerstl, Shane F.
Atty Docket : 1496.00053 / 00-487

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Manu Kashyap

9/23/05

Date


Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1621 Barber Lane, MS D-106
Milipitas, CA 95035
408-433-7475

Date: 9/23/05

Respectfully submitted,



Peter Scott

Reg. No. 33,279